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INPADOC

JP2000299360A2: SHEET-TYPE SEMICONDUCTOR IC WAFER DIRECT CONDUCTION **EMPERATURE-TESTING DEVICE** 

JP Japan Country:

Title:

A2 Document Laid open to Public inspection Kind:

**MORIWAKI IKURO** Inventor(s): **DOU YEE JAPAN CO LTD** 

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Oct. 24, 2000 / April 13, 1999 Issued/Filed Dates:

JP1999000140541 Application Number:

H01L 21/66 IPC Class: April 13, 1999 **JP1999000140541** Priority Number(s):

Abstract:

Problem to be solved: To perform day-to-day conduction high semiconductor IC wafer and the wafer probe pin module by an emperature shelf test at a low cost by applying pressure to a contacting direction, and by heating and cooling each of the semiconductor IC wafer and a wafer probe pin module in a ndividual temperature control system.

entatively locked by a chuck holder 4 and a probe pin module 2 are neating/ cooling conduction shelf test, thus easily performing day-toafter the entire probe pin 2 is brought into contact with the bump of are applied from a power supply/signal source 8 for carrying out a pinched between upper and lower parts by a heating block 3, and he wafer 1 to be inspected, a required power supply and a signal are further pressed by a press 7 so that the entire probe pin 2 is completely brought into contact with a wafer to be tested. Then, Solution: In a chamber 6, a wafer 1 to be inspected which is

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day conduction high temperature shelf test of many elements at a low cost. COPYRIGHT: (C)2000, JPO

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none Other Abstract Info:

No patents reference this one Foreign References:

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